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COMPUTER-AIDED DESIGN OF MICROSTRIP GaAs MESFET AMPLIFIERS

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ABSTRACT

Results on computer-aided design of broadband GaAs MESFET amplifiers in microstrip is presented. The analysis of an amplifier is based on measured scattering parameters and a model of the microstrip structure, which includes parasitics and junction effects. The optimized performance of one stage amplifiers with lossless distributed matching elements is presented. Realized amplifiers are in good agreement with the theory. One stage amplifiers with a 1 μm FET in chip form exhibit 5.8 dB of gain in the range 8-12 GHz, while a gain of 4.5 dB from 4-8 GHz has been obtained with a packaged 1 μm FET.

INTRODUCTION

This paper presents results on computer-aided design of broadband one stage amplifiers in microstrip with 1 μm-gate GaAs MESFET's and the measured performance of realized amplifiers. The scattering parameters of both packaged and chip transistors have been measured precisely by the use of microstrip standards. The amplifier network consists of lossless distributed matching elements as shunt stubs and coupled microstrip lines. The amplifier analysis incorporates microstrip junction effects and parasitics and the amplifiers are designed for a low VSWR at one port and a flat overall gain by selectively mismatching the other port with the aid of a minimax optimization routine.

DEVICE MOUNTING AND CHARACTERIZATION

The GaAs MESFET's are of the GAT 3 type from Plessey having a gatelength of 1 μm. In chip form the FET has been mounted on a disc (COD) in a drilled hole in a .635 mm thick alumina substrate. The GAT 3 is also available in a LID (P 102) package and packaged devices have been used in conjunction with a .38 mm thick duroid substrate ($\varepsilon_r = 2.4$).

Precise scattering parameter measurements have been performed by the use of a manual network analyzer and by off-line correction for connector and test equipment errors. This has been done by using microstrip reflection standards as a short, an open corrected for the end effect and a match realized by a 50 Ω chip resistor. Measured S parameters of a GAT 3 chip mounted on a COD in alumina substrate are shown in fig. 1 for a gate bias $V_{gs} = 0V$. The reference planes are at the beginning of the bond wire leading to the FET. The chip was potentially unstable up to 10.5 GHz having a calculated maximum available gain MAG of 8 dB at 12 GHz and a slope of nearly 5 dB pr. octave for the unilateral gain. A packaged device exhibited a calculated MAG of 9.6 dB at 4 GHz and MAG = 5.3 dB at 8 GHz.

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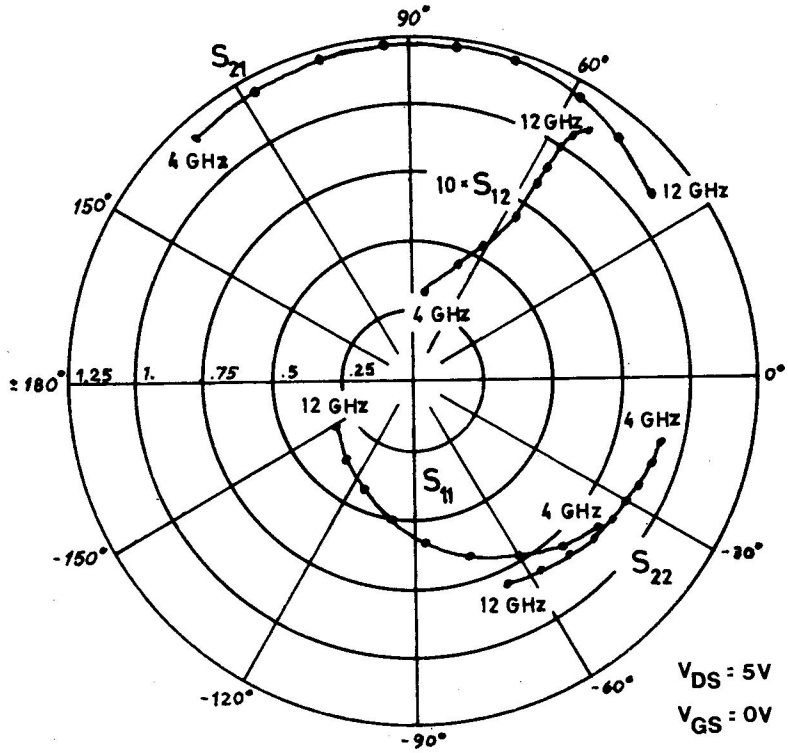

Fig. 1 Measured S parameters of a GAT 3 chip

AMPLIFIER DESIGN

It is preferable to design the input and output matching network of an one stage amplifier individually. By using a non-linear minimax optimization routine [1] one of the matching networks is designed for a low VSWR while the other is designed to exhibit a slope of the transmission that compensate the intrinsic gain taper of the FET. With both matching networks connected to the FET the overall gain has to be optimized for a flat response due to finite isolation of the FET. Distributed lossless microstrip elements as a transmission line, an open and short circuited stub and two coupled lines, where two opposite ports are open circuited, have been used. The description of these elements and the junction between them is based on equations presented in [2] - [4]. At the end of an amplifier design a more precise but also time consuming procedure can be used for analysis of the coupled lines.

Liechti and Tillman [5] have presented an excellent design method, where the matching for a low VSWR was obtained by $\lambda/4$ resonators coupled alternately by impedance and admittance inverters. A similar structure with $\lambda/2$ resonators coupled only by impedance inverters can also provide a good broadband match. The impedance inverters are realized by shorted shunt lines with a high characteristic impedance. In general an even better result can be obtained by using a structure of shunting parallel resonators and series resonators, realized by $\lambda/4$ short circuited shunt stubs coupled by $\lambda/4$ transmission lines. This structure leeds to physically large T-junction, which can be reduced by realizing a parallel resonator as two shorted shunt stubs in parallel or an $\lambda/2$ open circuited stub.

The structure with $\lambda/4$ resonators is also suitable for providing a prescribed transmission slope, such that the network is matched at the upper band

edge frequency and selectively mismatched at the lower edge. Shorted stubs enables the dc bias of the FET, while dc blocking can be obtained by replacing a series resonator by two coupled lines of a quarter wavelength, where two opposite ports are open circuited.

EXAMPLES OF BROADBAND AMPLIFIERS

In fig. 2 is shown the performance of a 8-12 GHz amplifier in alumina with a GAT-3 chip. The input is matched by one $\lambda/2$ resonator and two impedance inverters, while the output compensates the gain taper by a high impedance line to resonate the output of the FET, a shunt resonator and one transformer (fig. 2b). A gain of 5.8 dB ±.1 dB has been obtained. Fig. 3 shows the best result obtained with the shunting parallel resonator structure. As the input of the FET (fig. 1) is nearly resonated at 12 GHz the first T-junction degrades the performance of this structure. The measured performance of a realized amplifier is also shown (fig. 3a) and a fine agreement has been obtained. The deviation is mainly due to a shorter drain bonding wire in the realized amplifier.

For a 4-8 GHz amplifier with a packaged GAT 3 the best result was obtained by the structure with parallel shunt resonators. A gain of 4.5 dB ± .2 dB and an output VSWR less than 2.6 has been realized. The calculated and measured performance is shown in fig. 4 together with the structure of the amplifier circuit. An excellent agreement between theory and the measurements has been obtained. If the transmission line in the output network of the amplifier in fig. 4b is replaced by two coupled lines (fig. 5b) to provide a dc block a similar theoretical performance can be obtained (fig. 5a).

CONCLUSION

One stage MESFET amplifiers in microstrip have been designed by a computer-aided technique, where junction effects and parasitics in the network structure is taken into account. The measured performance of realized untuned amplifiers is in good agreement with the theory. This shows the feasibility of making reproducible designs of broadband multi stage amplifiers.

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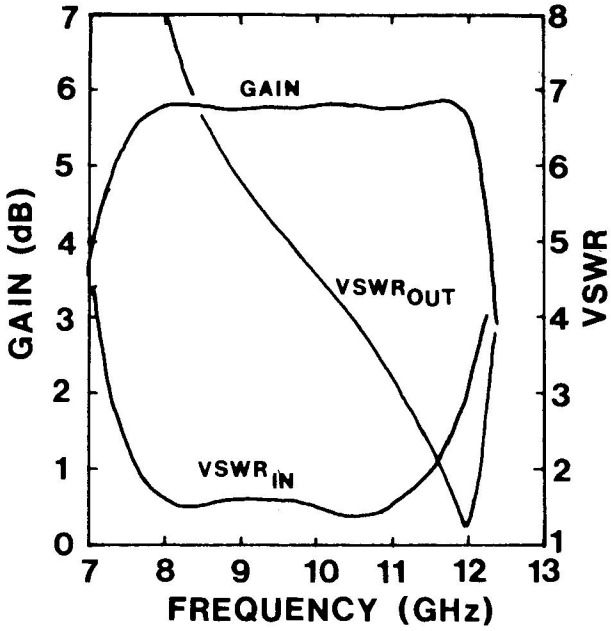

FIG 2a

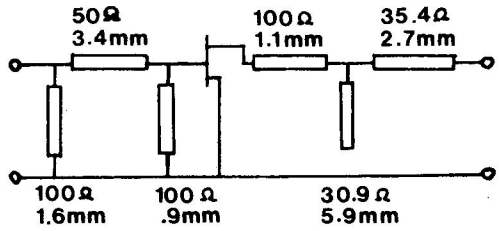

FIG 2b

Fig. 2(a) Power gain and VSWR's of an X-band amplifier with one GAT 3 chip.
(b) The amplifier circuit.

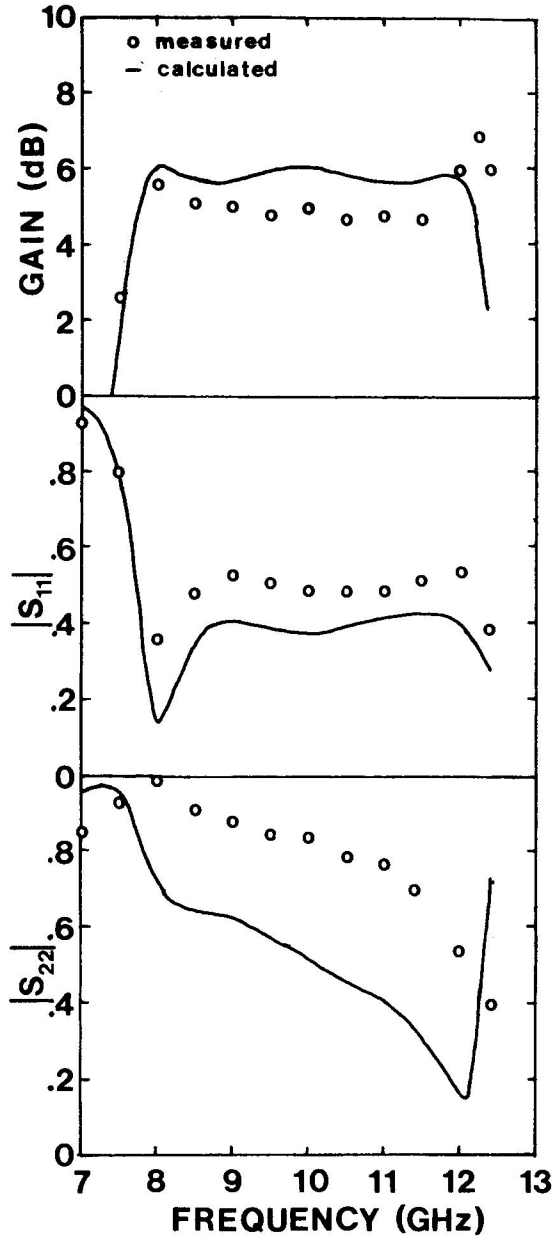

FIG 3a

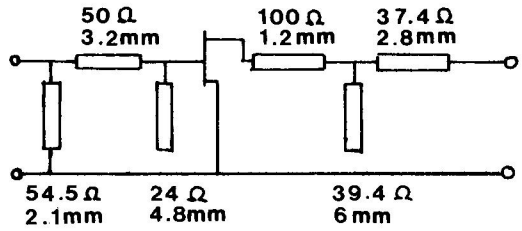

FIG 3b

Fig. 3(a) Measured and calculated performance of an X-band amplifier with one GAT 3 chip.
(b) The amplifier circuit.

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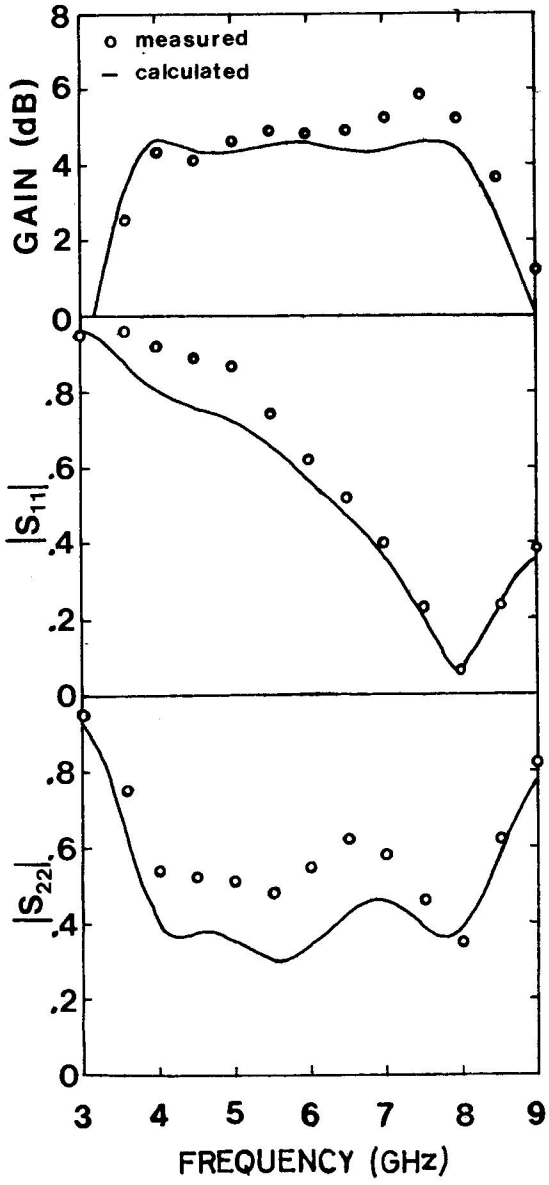

FIG 4a

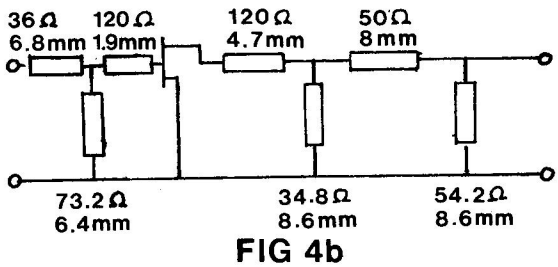

FIG 4b

Fig. 4(a) Measured and calculated performance of a C-band amplifier with a LID packaged GAT 3.
(b) The amplifier circuit.

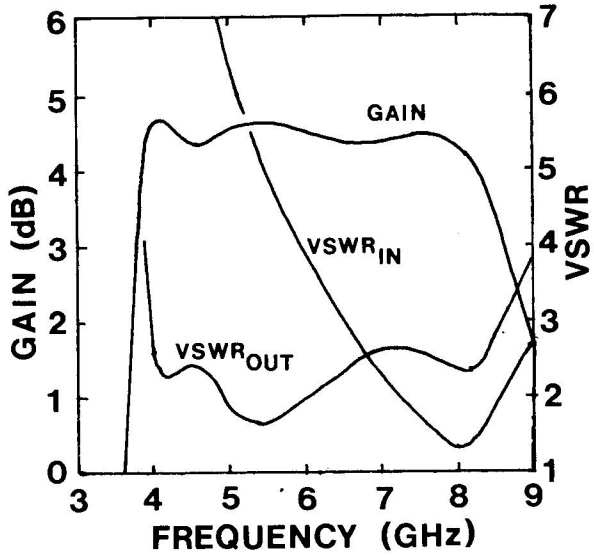

FIG 5a

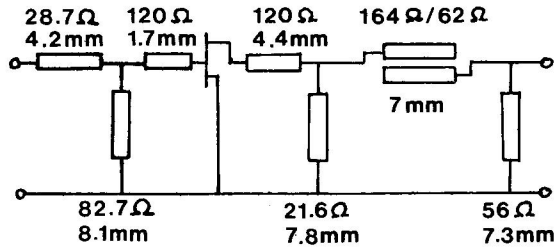

FIG 5b

Fig. 5(a) Power gain and VSWR's of a C-band amplifier with a LID packaged GAT 3.
(b) The amplifier circuit.